



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

2

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/460,898	12/14/1999	NAOKI MATSUOKA	FUJY-16.847	3089

7590 04/14/2005

HELFGOTT & KARAS
575 MADISON AVENUE
FLOOR 26
NEW YORK, NY 10022-8508

EXAMINER

LAFORGIA, CHRISTIAN A

ART UNIT	PAPER NUMBER
----------	--------------

2131

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/460,898

Applicant(s)

MATSUOKA ET AL.

Examiner

Christian La Forgia

Art Unit

2131

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) 23 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-22, 24, 26-28, 31, 32, 36-38 and 40 is/are allowed.
- 6) ☒ Claim(s) 25, 29, 30, 33-35 and 39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 December 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Art Unit: 2131

DETAILED ACTION

1. The amendment filed on 16 December 2004 has been noted and made of record.
2. Claims 1-40 have been presented for examination.
3. Claim 23 has been cancelled as per Applicant's request.
4. Claims 1-22, 24, 26-28, 31, 32, 36-38 and 40 are allowed.

Response to Arguments

5. Applicant's arguments, see pages 28-30, filed 16 December 2004, with respect to claims 1-22, 24, 26-28, 31, 32, 36-38 and 40 have been fully considered and are persuasive. The rejection of claims 1-22, 24, 26-28, 31, 32, 36-38 and 40 has been overcome.
6. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies, such as a scheduling unit that handles arbitration between input lines that does not result in competition, are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
7. See further rejections that follow.

Claim Rejections

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Art Unit: 2131

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claims 25, 33-35, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,449,283 to Chao et al., hereinafter Chao, in view of United States Patent No. 6,262,986 to Oba et al., hereinafter Oba.

11. As per claim 25, Chao teaches a scheduling control system for a switch having a Virtual Output Queue comprising:

a request information management unit managing the number of scheduling requests and holding forwarding request information on each input line as a scheduling target with respect to a desired output line (Figures 7a [block 714], 7b [block 714'], 8 [block 810, 840], 10 [blocks 1010, 1020, 1030, 1040], 11, 12 [blocks 1250, 1260, 1262, 1270], 13 [block 1270'], 15 [block 1520], 16 [blocks 1630, 1640], 17, 20a, 20b, 28, 37a, 37b, 37c; column 7, lines 33-44; column 8, lines 10-47; column 10, lines 27-50; column 12, lines 38-51; column 17, lines 22-29);

a priority pointer control unit for indicating a start number of the priority patterns (Figure 33; column 31, lines 20-48; column 31, line 51 to column 32, line 52),

wherein the scheduling processing unit sequentially performs the scheduling for the N-patterns from the priority pattern indicated by a priority pointer, and updates the start number of the priority patterns at a next scheduling cycle (Figure 33; column 21, lines 22-48; column 30, lines 19-56; column 31, lines 20-48; column 31, line 51 to column 32, line 52).

12. Chao does not teach a scheduling processing unit, having N-pieces (N is a natural number equal to or more than 2) of priority patterns with different selection priorities between the

Art Unit: 2131

respective output lines, for selecting the output line unused by other input lines in accordance the priority pattern and the forwarding request information.

13. Oba teaches a scheduling processing unit, having N-pieces (N is a natural number equal to or more than 2) of priority patterns with different selection priorities between the respective output lines, for selecting the output line unused by other input lines in accordance the priority pattern and the forwarding request information (Figures 1 [block 16], 2 [block 16], 3, 4, 5a [block 16], 5b [block 16], 8a-d [block 16], 10 [blocks 11-1, 11-2, 11-N], 13; column 4, line 62 to column 6, line 53; column 7, line 49 to column 8, line 29; column 12, line 44 to column 13, line 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the scheduling processing unit of Oba with the system of Chao, as it would create a system in which all packets were dealt with fairly. One would be motivated to combine such a scheduling unit in the system of Chao as it would ensure that the use of bandwidth was being maximized as well as creating a method in which delivery was ensured via quality of service techniques as discussed both in Chao and Oba.

14. Regarding claim 33, Chao teaches a packet switching method for a switch having a Virtual Output Queue comprising the steps of:

imparting a sequence number to a phase-synchronization-oriented cell transferred from each input line (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33);

Art Unit: 2131

sequentially incrementing the output line number (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33);

shifting the output line number at the same timing between the respective input lines (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33); and,

executing phase synchronization at a cell level by comparing a timing of receiving the phase-synchronization-oriented cell with the sequence number at each lattice point on the switch side (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33).

15. Chao does not teach in a scheduling process of updating an inter-highway pointer indicating a start-of-scheduling input line to a next adjacent input line at every scheduling cycle, and updating an intra-highway pointer indicating a start-of-retrieval output line to a line adjacent to the line with the forwarding determined on the basis of forwarding request information corresponding to the input line.

16. Oba teaches in a scheduling process of updating an inter-highway pointer indicating a start-of-scheduling input line to a next adjacent input line at every scheduling cycle, and updating an intra-highway pointer indicating a start-of-retrieval output line to a line adjacent to the line with the forwarding determined on the basis of forwarding request information corresponding to the input line (Figures 1 [block 16], 2 [block 16], 3, 4, 5a [block 16], 5b [block 16], 8a-d [block 16], 10 [blocks 11-1, 11-2, 11-N], 13; column 4, line 62 to column 6, line 53; column 7, line 1 to column 10, line 3). Therefore it would have been obvious to one of ordinary

Art Unit: 2131

skill in the art at the time the invention was made to include the scheduling processing unit of Oba with the system of Chao, as it would create a system in which all packets were dealt with fairly. One would be motivated to combine such a scheduling unit in the system of Chao as it would ensure that the use of bandwidth was being maximized as well as creating a method in which delivery was ensured via quality of service techniques as discussed both in Chao and Oba.

17. As per claim 34, Chao teaches a packet switching method for a switch having a Virtual Output Queue comprising the steps of:

transferring in broadcast the cells given the sequence numbers to respective lattice points within the switch from the respective input lines (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33); and,

executing phase synchronization at a cell level by comparing the sequence numbers of the arrived cells at the lattice points within the switch (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33).

18. Chao does not teach a scheduling process of updating an inter-highway pointer indicating a start-of-scheduling input line to a next adjacent input line at every scheduling cycle, and updating an intra-highway point indicating a start-of-retrieval output line to a line adjacent to the line with the forwarding determined on the basis of forwarding request information corresponding to the input line.

19. Oba teaches in a scheduling process of updating an inter-highway pointer indicating a start-of-scheduling input line to a next adjacent input line at every scheduling cycle, and updating an intra-highway point indicating a start-of-retrieval output line to a line adjacent to the

Art Unit: 2131

line with the forwarding determined on the basis of forwarding request information corresponding to the input line (Figures 1 [block 16], 2 [block 16], 3, 4, 5a [block 16], 5b [block 16], 8a-d [block 16], 10 [blocks 11-1, 11-2, 11-N], 13; column 4, line 62 to column 6, line 53; column 7, line 1 to column 10, line 3). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the scheduling processing unit of Oba with the system of Chao, as it would create a system in which all packets were dealt with fairly. One would be motivated to combine such a scheduling unit in the system of Chao as it would ensure that the use of bandwidth was being maximized as well as creating a method in which delivery was ensured via quality of service techniques as discussed both in Chao and Oba.

20. With regards to claim 35, Chao teaches a packet switching method for a switch having a Virtual Output Queue comprising the steps of:

transferring the cells to the respective lattice points within the switch from the input lines (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33); and,

adjusting a phase difference at a cell level by a phase adjustment buffer provided at each lattice point (Figure 13 [blocks 1320, 1350, 1370], 36a, 36b, 36c; column 18, line 28 to column 19, line 12; column 31, line 51 to column 32, line 33).

21. Chao does not teach in a scheduling process of updating an inter-highway pointer indicating a start-of-scheduling input line to a net adjacent input line at every scheduling cycle, and updating an intra-highway pointer indicating a start-of-retrieval output line to a line adjacent

Art Unit: 2131

to the line with the forwarding determined on the basis of forwarding request information corresponding to the input lines.

22. Oba teaches in a scheduling process of updating an inter-highway pointer indicating a start-of-scheduling input line to a net adjacent input line at every scheduling cycle, and updating an intra-highway pointer indicating a start-of-retrieval output line to a line adjacent to the line with the forwarding determined on the basis of forwarding request information corresponding to the input lines (Figures 1 [block 16], 2 [block 16], 3, 4, 5a [block 16], 5b [block 16], 8a-d [block 16], 10 [blocks 11-1, 11-2, 11-N], 13; column 4, line 62 to column 6, line 53; column 7, line 1 to column 10, line 3). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the scheduling processing unit of Oba with the system of Chao, as it would create a system in which all packets were dealt with fairly. One would be motivated to combine such a scheduling unit in the system of Chao as it would ensure that the use of bandwidth was being maximized as well as creating a method in which delivery was ensured via quality of service techniques as discussed both in Chao and Oba.

23. Regarding claim 39, Chao does not teach wherein the scheduling processing unit applies a random array of inverted LSB/MSB of binary notation permutation layout patterns as the above priority patterns.

24. Oba teaches wherein the scheduling processing unit applies a random array of inverted LSB/MSB of binary notation permutation layout patterns as the above priority patterns (Figures 7, 8A, 8B, 8C, & 8D; column 11, line 22 to column 12, line 3; column 12, line 44 to column 13, line 25). It would have been obvious to one of ordinary skill of the art at the time the invention

Art Unit: 2131

was made to invert the binary notation of Oba as simply reversing or rearranging parts. See *In re Japikse*, 181 F.2d 1019, 1023, 86 USPQ 70, 73 (CCPA 1950).

25. Claims 29 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Chao.

26. As per claim 29, Chao teaches a packet switch having a Virtual Output Queue comprising:

sorters each serving as a unit sorter for sorting input cells coming from m-lines of input routes and transferring the sorted input cells to m-lines of output routes, the packet switch being constructed by connecting the unit sorters at multi-stages (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23),

wherein outputs per the unit sorter of a first-stage unit sorter group are outputted separately to a dummy sorter provided at a second stage and the unit sorter at the second stage (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23), and,

outputs of the second-stage dummy sorter and of the second-stage unit sorter are inputted to a third-stage unit sorter group (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23).

N-input/N-output sorter network is configured on the whole by connecting $(2N/m-1) * N/m$ pieces of the unit sorters (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23). See MPEP 716.01(a) concerning $(2N/m-1) * N/m$.

Art Unit: 2131

27. Regarding claim 30, Chao teaches a packet having a Virtual Output Queue comprising: sorters each serving as a unit sorter for sorting input cells coming from m-lines of input routes and transferring the sorted input cells to N-lines of output routes, the packet switch being constructed by connecting the unit sorters at multi-stages in matrix X- and Y-directions (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23);

wherein outputs of the respective unit sorters are inputted to next-stage unit sorters positioned in (+)X- and (-)Y-directions of the unit sorter (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23),

when extending the sorter group, the outputs of the respective unit sorters are inputted next-stage unit sorters positioned in the (+)X-direction of the unit sorter (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to column 26, line 20; column 28, lines 1-23), and

an N-input/N-output sorter network is configured on the whole by connecting $N/m \cdot (N/m+1)/2$ pieces of the unit sorters (Figures 18 & 32; column 20, line 38 to column 21, line 49; column 24, lines 7-48; column 24, line 64 to 26, line 20; column 28, lines 1-23). See MPEP 716.01(a) concerning $(2N/m-1) \cdot N/m$.

Allowable Subject Matter

28. The following is an examiner's statement of reasons for allowance:

Art Unit: 2131

The amendments made to the independent claims were sufficient to overcome the prior art. After further consideration and an updated search, the Examiner was unable to find relevant prior art or any motivation to modify the reference in a manner similar to the instant invention, therefore the claims indicated above are in condition for allowance.

29. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

30. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

31. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (571) 272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

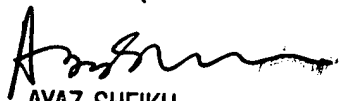
Art Unit: 2131

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian LaForgia
Patent Examiner
Art Unit 2131

clf


AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100